

**REMARKS**

Claims 1–23 are pending in the present application.

Claims 7–20 are allowed; claim 23 was indicated to be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims. .

Claim 23 has been amended to be rewritten in independent form including all limitations of the base claim and any intervening claims..

Reconsideration of the claims is respectfully requested.

**35 U.S.C. § 102 (Anticipation)**

Claims 1–6 and 21–22 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,526,391 to *Shankar et al.* This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-76 (8<sup>th</sup> ed. rev. 3 August 2005).

Independent claims 1 and 12–22 each recite that the set of logic gates receive the input signal and produce the output signal. Such a feature is not found in the cited reference. The control logic of Figure 2 in *Shankar et al* receives the output signal OUT (from N+1 counter 20 in Figure 1) as an input, rather than producing that signal as an output as recited in the claims.

Therefore, the rejection of claims 1–6 and 21–22 under 35 U.S.C. § 102 has been overcome.


If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@munckbutrus.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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